अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन जरनल, मार्च 2023
The Semiconductor Integrated Circuits Layout Design Journal, March 2023

भारत सरकार

अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री

Government of India

The Semiconductor Integrated Circuits Layout Design Registry

निर्गमन सं **137/2023**	शुक्रवार	दिनांक:**10/03/2023**
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अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन अधिनियम, 2000 के अधीन प्रकाशित

रजिस्ट्रार कार्यालय, अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री, भारत सरकार

Published under Semiconductor Integrated Circuits Layout Design Act, 2000

Government of India, Office of the Registrar, Semiconductor Integrated Circuits Layout Design Registry,

वाणिज्य एवं उद्योग मंत्रालय

Ministry of Commerce and Industry

बौद्धिक संपदा भवन

Boudhik Sampada Bhawan

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अनुक्रमणिका
INDEX

प्रस्तावना

अर्धचालक एकीकृत परिपथ अभिन्या सडिज़ाइन रजिस्ट्री 1 मई, 2011 से सेमीकंडक्टर एकीकृत परिपथ अभिन्यास डिज़ाइन अधिनियम, 2000 के अतंर्गत चालू की गई है । अधिनियम के अतंर्गत प्रावधानों के अनुसार अर्धचालक एकीकृत परिपथ अभिन्यास डिज़ाइन जनरल का प्रकाशन अपेक्षित है । इस जनरल का प्रकाशन महीने के दूसरे शुक्रवार कार्य दिवस पर किया जाएगा । इस जनरल से संबंधित सभी पूछ-ताछ अथवा कोई भी अन्य अपेक्षित सूचना रजिस्ट्रार, अर्धचालक एकीकृत परिपथ अभिन्यास डिज़ाइन रजिस्ट्री को संबोधित की जा सकती है । किसी भी प्रकार के सुझावों तथा टिप्पणियों का स्वागत है ।

(प्रो. (डॉ.) उन्नत पी. पंडित)
रजिस्ट्रार

INTRODUCTION

The Semiconductor Integrated Circuits Layout-Design Registry has been made operational w.e.f. 1st May 2011 under the Semiconductor Integrated Circuits Layout-Design Act, 2000. In accordance with the provisions under the Act "The Semiconductor Integrated Circuits Layout-Design Journal" is required to be published. This Journal is being published on the 2nd working Friday of the month. All the enquiries related to this Journal or any other information as required should be addressed to the Registrar, Semiconductor Integrated Circuits Layout-Design Registry. Any suggestions and comments are welcome.

(Prof. (Dr) Unnat P. Pandit)
REGISTRAR

क. आधिकारिक टिप्पणियां

A. Official Notes

अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन आवेदन के पंजीकरण से संबंधित कोई भी जानकारी सभी कार्य-दिवसों में अपराह्न 3.00 से 4.00 के बीच प्राप्त की जा सकती है ।

(प्रो. (डॉ.) उन्नत पी. पंडित)
रजिस्ट्रार

All the queries relating to registration of Semiconductor Integrated Circuits Layout Design may be obtained from the Registry between Timing 3:00 PM to 4.00 PM all working days.

(Prof. (Dr) Unnat P. Pandit)
REGISTRAR

ख. अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री कार्यालय का अधिकार क्षेत्र

B. Jurisdiction of Office of the Semiconductor Integrated Circuits Layout Design Registry

अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री (एस. आई. सी. एल. डी. आर.) का मुख्य कार्यालय, बौद्धिक संपदा भवन, प्लॉट नं ३२, सेक्टर १४, द्वारका, नई दिल्ली – 110075 में स्थित है । इसकी ऱाज्यक्षेत्रीय परिसीमाएं जिसके भीतर अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री का कार्यालय अपने कृत्य कर सकेगा, सम्पूर्ण भारत पर है ।

(प्रो. (डॉ.) उन्नत पी. पंडित)
रजिस्ट्रार

The Semiconductor Integrated Circuits Layout-Design Registry (SICLDR) has its head office located in the Boudhik Sampada Bhawan, Plot no. 32, Sector – 14, Dwarka, New Delhi-110075. The territorial limits within which such office of the Semiconductor Integrated Circuits Layout-Design Registry may exercise its functions shall be the whole of India.

(Prof. (Dr) Unnat P. Pandit)
REGISTRAR

ग. स्वीकृति के पश्चात विज्ञापित आवेदन – तीन*

C. Applications advertised after acceptance – Three*

Application Received for Registration under Semiconductor Integrated Circuits Layout Design Act 2000

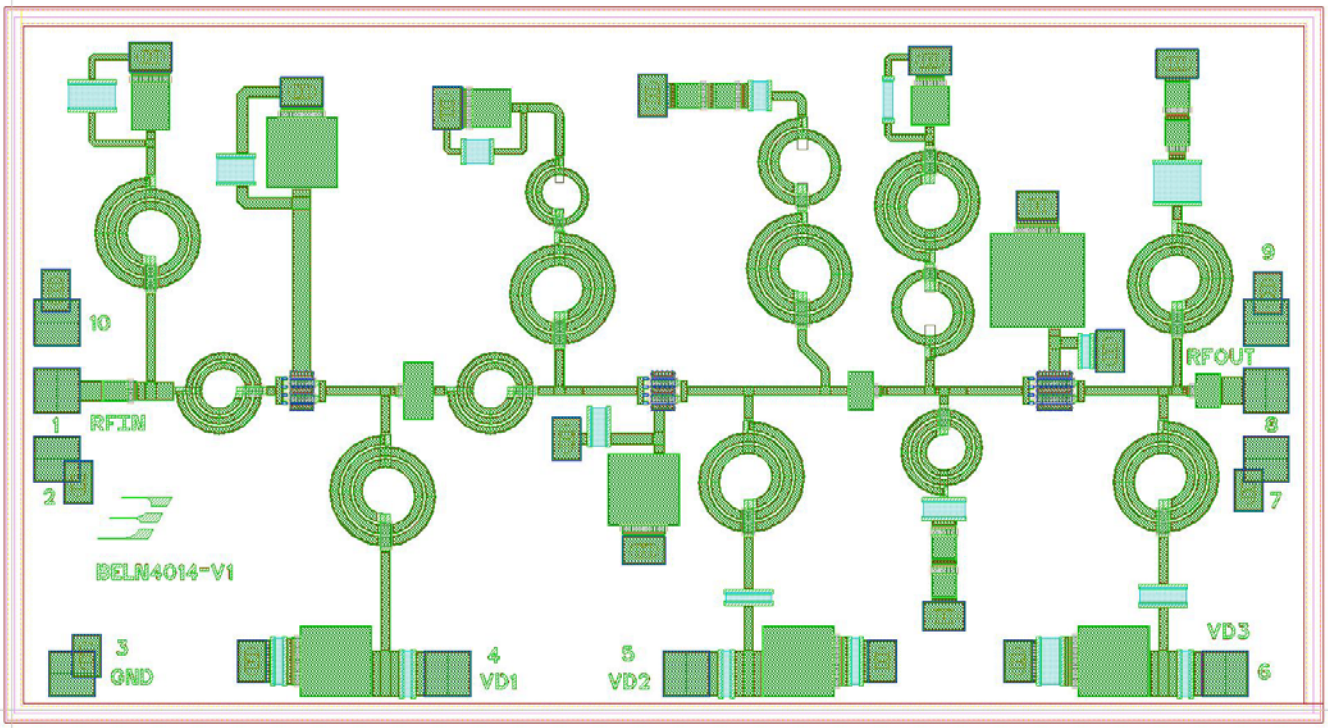
Semiconductor Integrated Circuits Layout Design (SICLD) Registry has received an application for registration of ULTRA-HIGH GAIN AND LOW NOISE MONOLITHIC X BAND MMIC AMPLIFIER ON 0.15 UM INGAAS PROCESS, Application no: LD-1/9/2020 in the name of M/s Bharat Electronics Limited, c/o Bharat Electronics Limited, Corporate Office, Outer Ring Road, Nagavara, Bangalore-560045, India. Details of the applications are as below:

1. **Date of Receipt for registration of layout design**: 05/06/2020.
2. **Brief Description of the layout design:** The present layout has three amplifying stages of X band low noise amplifier with a die size of 2.8umX 1.5um fabricated on 0.1um InGaAs substrate and with 0.15umgate length process. It is a monolithic, self-biased, single supply, 3 stage low noise amplifier with high gain and low noise figure consisting of input matching network, stage l, inter-stage matching network between first and second stage, stage2, inter-stage matching network between second and third stage, stage 3 and output matching network. The LNA operates in the frequency range of 8.5GHz to 10.5GHz with a gain of 29dB and noise figure of 1.1dB over the frequency band.
3. **Whether the layout design has been commercially exploited:** No
4. **The Address of the office of the registry where the application is filed:** SICLD Registry, Boudhik Sampada Bhawan, Plot No. 32, Sector-14,Dwarka, New Delhi - 110078.

Anyone willing to oppose the filing of the application by M/s Bharat Electronics Limited, c/o Bharat Electronics Limited, Corporate Office, Outer Ring Road, Nagavara, Bangalore-560045, India, may kindly send their application to the SICLD Registry Boudhik Sampada Bhawan, Plot No. 32, Sector-14,Dwarka, New Delhi - 110078.

A notice of opposition to the registration of a layout design under sub section (1) of section 11 shall be given in triplicate on Form LD-2 accompanied by prescribed fee within three months from the date of advertisement of the application for registration in the journal (www.sicldr.gov.in). The notice shall include a statement of the grounds on which the opponent objects to the registration.

To obtain details how to apply, please visit website: www.sicldr.gov.in
Duly filled Application Form may please be sent to: **Registrar**
Semiconductor Integrated Circuits Layout Design Registry, Department for Promotion of Industry and Internal Trade, Ministry of Commerce & Industry (Government of India)
Boudhik Sampada Bhawan, Plot No. 32, Sector-14,
Dwarka, New Delhi - 110078



1. 4X 50 umpHEMT Device,
2. 2-4 X 50umpHEMT Device,
3. 4X 75um Device,
4. Foundry modelled round inductor,
5. Thin film resistor,
6. MIM Capacitor,
7. RF Input bond pad,
8. Back side via for grounding,
9. DC bond pad, and
10. RF output bond pad

Application Received for Registration under Semiconductor Integrated Circuits Layout Design Act 2000

Semiconductor Integrated Circuits Layout Design (SICLD) Registry has received an application for registration of HIGH GAIN AND ULTRA-LOW NOISE C BAND AMPLIFIER, Application no: LD-1/10/2020 in the name of M/s Bharat Electronics Limited, c/o Bharat Electronics Limited, Corporate Office, Outer Ring Road, Nagavara, Bangalore-560045, India. Details of the applications are as below:

1. **Date of Receipt for registration of layout design**: 09/06/2020.
2. **Brief Description of the layout design:** Brief Description of the Layout-Design: This layout relates to a C-Band-microwave frequency range self-biasedtwo stage low noise amplifier (LNA) with high gain and ultra-low noise using InGaAstechnology to achieve smaller die size, low noise figure and high gain. The present layout is a two-stage low noise amplifier with die dimensions of 1.5X1.5X0.1 millimeter in X, Y and Z directions. It is designed and fabricated on 0.15 micro meter gate length process. All the resistors (Starts with letter R) are implemented using Thin Film Resistors(TFR).All the capacitors(Starts with letter C) are implemented usingMIM (Metal Insulator Metal). All inductors (Starts with letter L) use air bridges for cross connections.
3. **Whether the layout design has been commercially exploited:** No
4. **The Address of the office of the registry where the application is filed:** SICLD Registry, Boudhik Sampada Bhawan, Plot No. 32, Sector-14,Dwarka, New Delhi - 110078.

Anyone willing to oppose the filing of the application by M/s Bharat Electronics Limited, c/o Bharat Electronics Limited, Corporate Office, Outer Ring Road, Nagavara, Bangalore-560045, India, may kindly send their application to the SICLD Registry Boudhik Sampada Bhawan, Plot No. 32, Sector-14,Dwarka, New Delhi - 110078.

A notice of opposition to the registration of a layout design under sub section (1) of section 11 shall be given in triplicate on Form LD-2 accompanied by prescribed fee within three months from the date of advertisement of the application for registration in the journal (www.sicldr.gov.in). The notice shall include a statement of the grounds on which the opponent objects to the registration.

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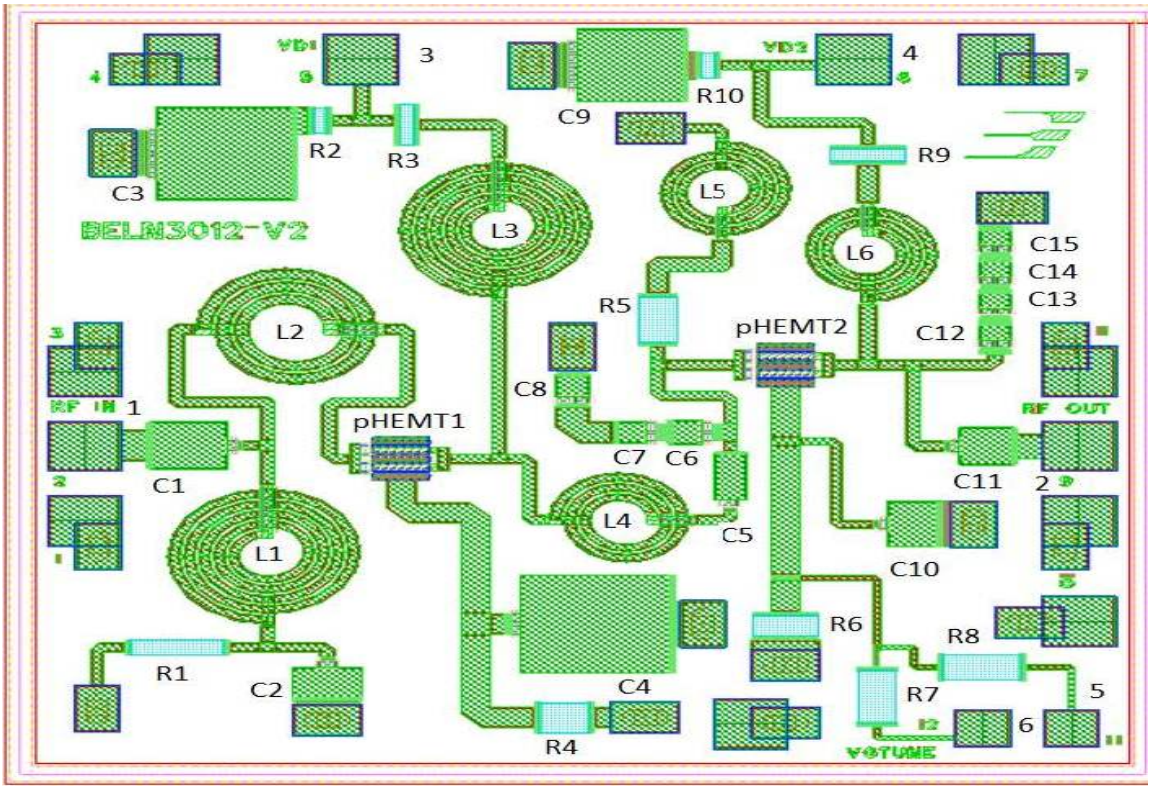
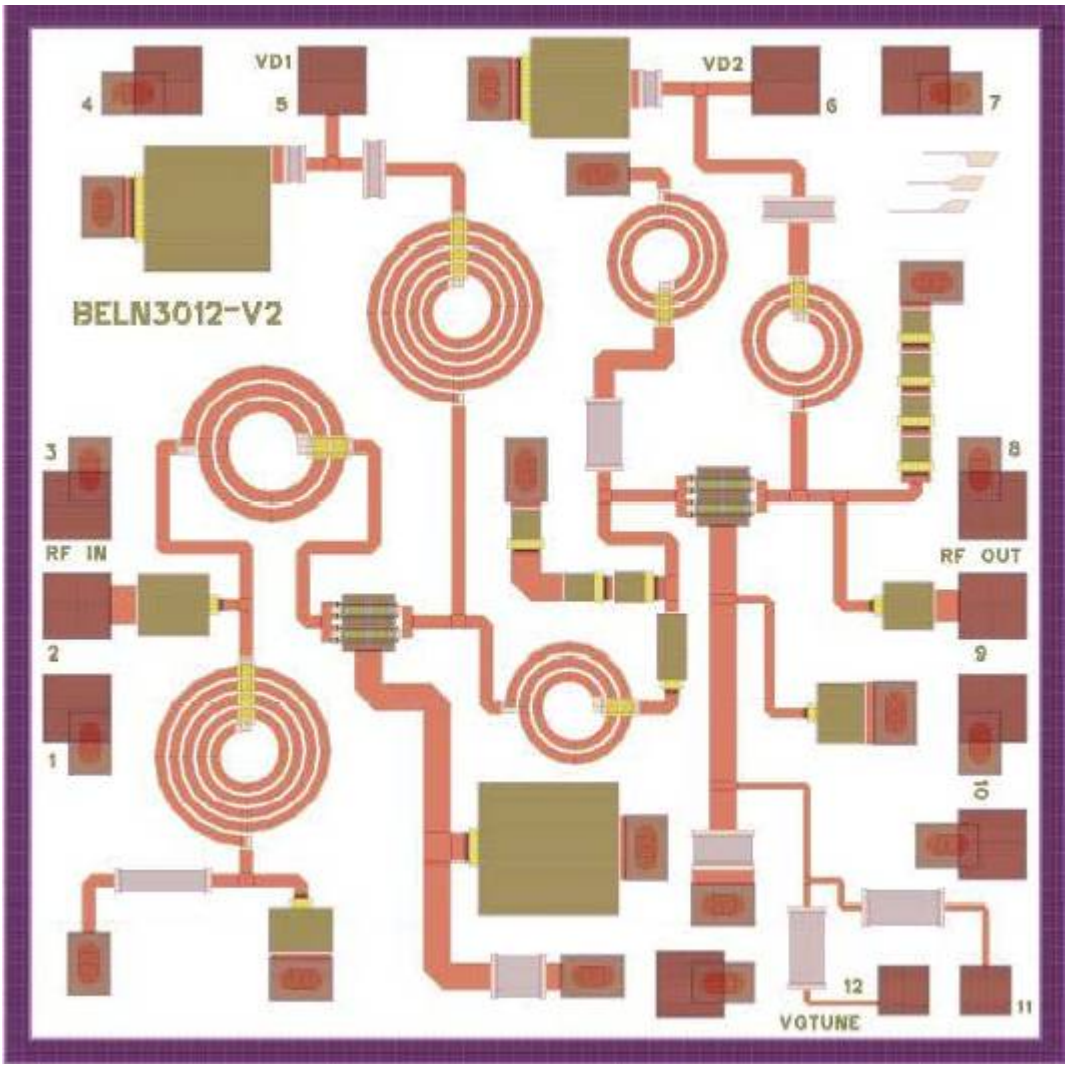
Dwarka, New Delhi - 110078



The pHEMT (Pseudomorphic high electron mobility transistors) (name das pHEMT1 and pHEMT2) have gate periphery of 4X75 micro meter. 1& 2 are RF in and RF out, 3 & 4 are supply pads, 5&6 are gate control pads respectively.


VD1
VD2
4
5
6
7
BELN3012-V2
3
RF IN
2
1
8
RF OUT
9
10
12
11
VGTUNE

Application Received for Registration under Semiconductor Integrated Circuits Layout Design Act 2000

Semiconductor Integrated Circuits Layout Design (SICLD) Registry has received an application for registration of S BAND 8-BIT DIGITALPHASE SHIFTER, Application no: LD-1/11/2020 in the name of M/s Bharat Electronics Limited, c/o BharatElectronics Limited, Cornorate Oficc. Outer Ring Road. Nagavara Bangalore-560045. Details of the applications are as below:

1. **Date of Receipt for registration of layout design**: 08/12/2020.
2. **Brief Description of the layout design:** This layout relates to an S-band 8-bit digital phase shifter with phase resolution of 1.4°. It is designed using 0.25um InGaAs (Indium Gallium Arsanide) pHEMT technology to achieve low insertion loss, low RMS phase error, high linearity and low current consumption. The S band 8-bit digital phase shifter MMIC layout dimension is 5.3 X 2.5 X 0.1 millimeters in X, Y and Z directions. All the switch transistors (Starts with letter T) are implemented using D2-process P-N junction switches, resistors (Starts with letter R) are implemented using EPR, capacitors (Starts with letter C) are implemented using MIM (Metal Insulator Metal) and inductors (Starts with letter L) implemented using scalable spiral round inductors.
3. **Whether the layout design has been commercially exploited:** No
4. **The Address of the office of the registry where the application is filed:** SICLD Registry, Boudhik Sampada Bhawan, Plot No. 32, Sector-14,Dwarka, New Delhi - 110078.

Anyone willing to oppose the filing of the application by M/s Bharat Electronics Limited, c/o Bharat Electronics Limited, Corporate Office, Outer Ring Road, Nagavara, Bangalore-560045, India, may kindly send their application to the SICLD Registry Boudhik Sampada Bhawan, Plot No. 32, Sector-14,Dwarka, New Delhi - 110078.

A notice of opposition to the registration of a layout design under sub section (1) of section 11 shall be given in triplicate on Form LD-2 accompanied by prescribed fee within three months from the date of advertisement of the application for registration in the journal (www.sicldr.gov.in). The notice shall include a statement of the grounds on which the opponent objects to the registration.

To obtain details how to apply, please visit website: www.sicldr.gov.in
Duly filled Application Form may please be sent to: **Registrar**
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Dwarka, New Delhi - 110078

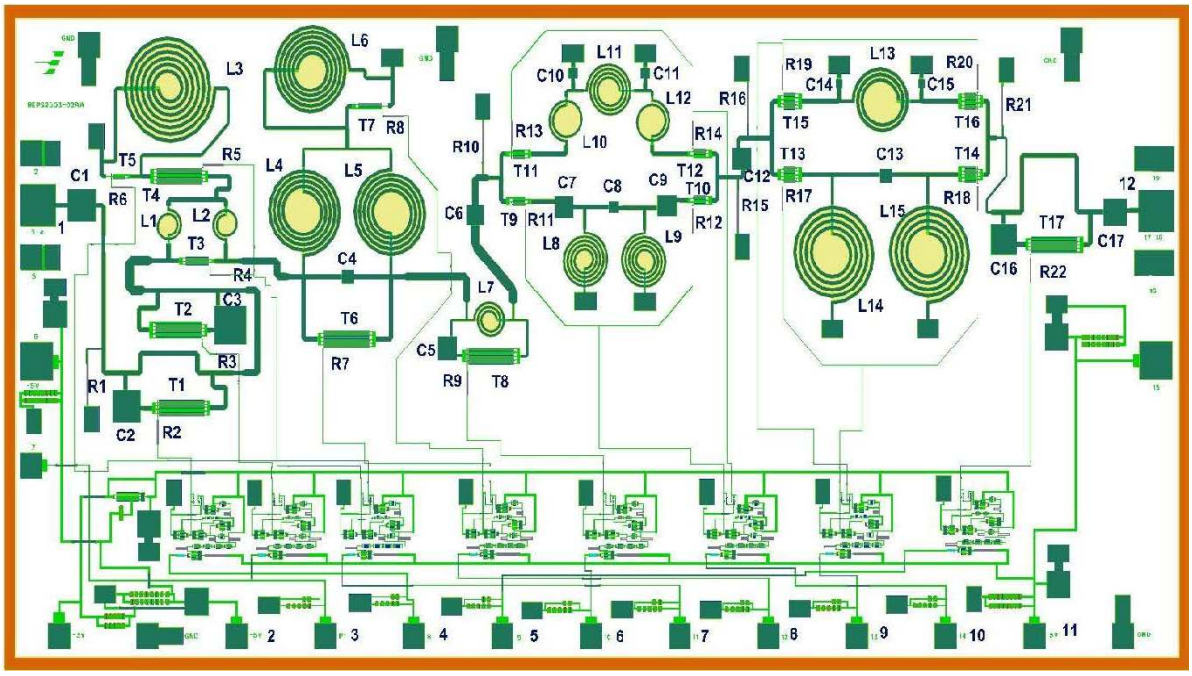
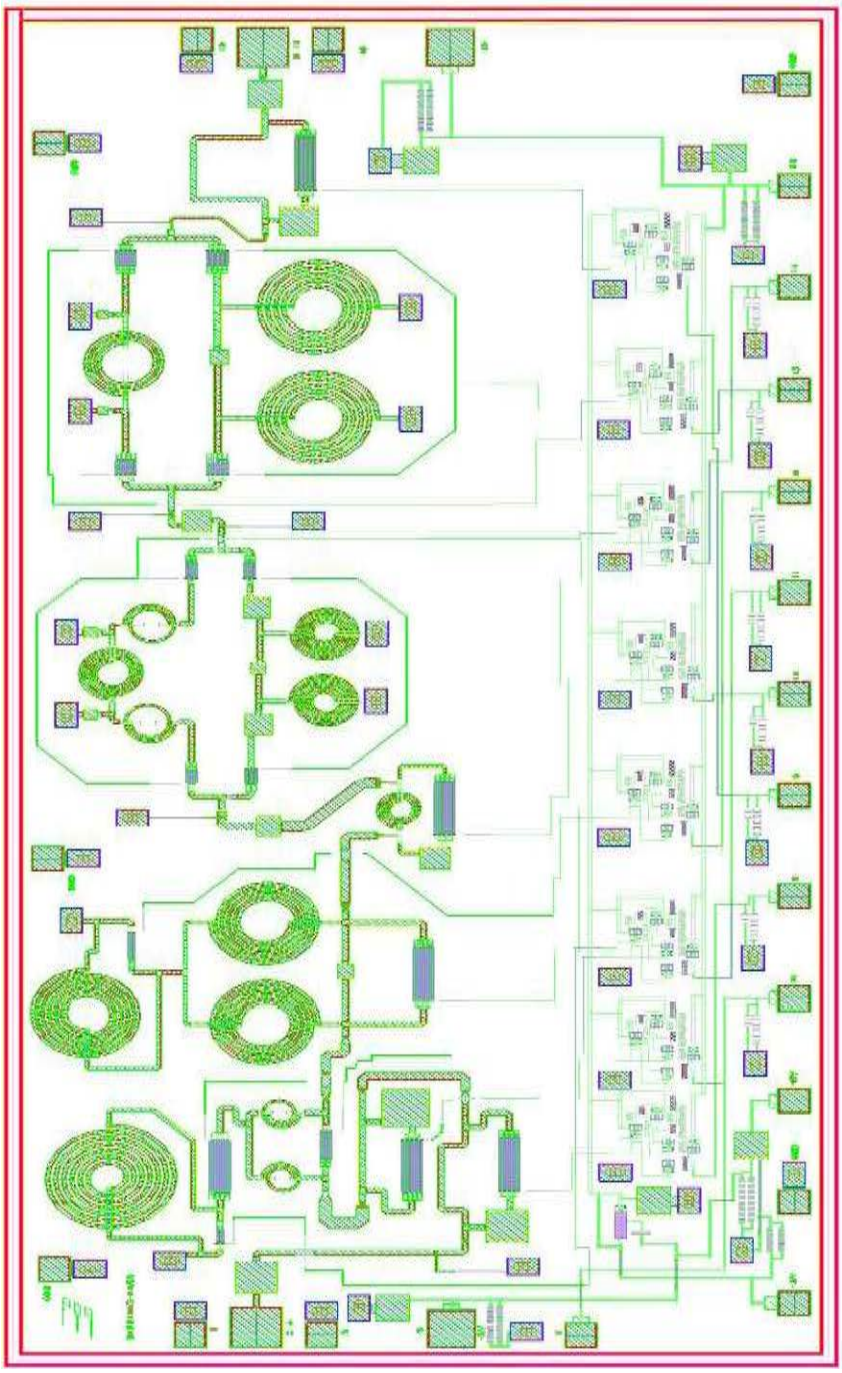
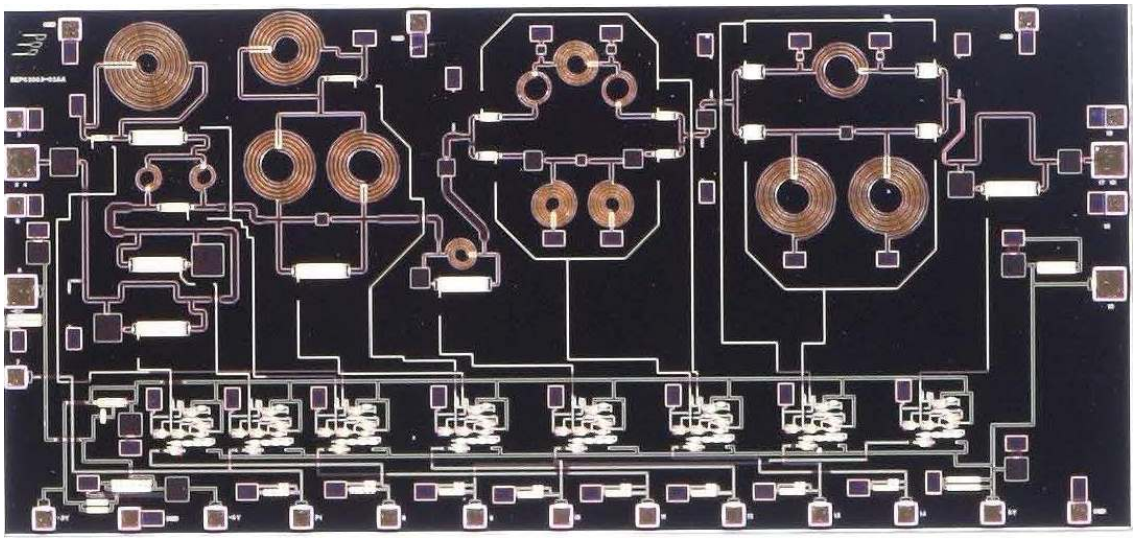


Fig 1. S band 8-bit digital phase shifter

As shown in Figure 1, Pad numbers 1 & 12 represents is RF input & RF outputs respectively, 2 & 11 represents power supply pads and numbers 3 to 10 represents TTL control input pads.





*तीन आवेदन प्राप्त हुआ।
**three application received.*

घ. आवेदन में शुध्दि या संशोधन करने की अधिसूचना - शून्य

D. Notification of correction or amendment of application - Nil