

अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन जरनल, जुलाई 2023
The Semiconductor Integrated Circuits Layout Design Journal, July 2023

भारत सरकार
अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री
Government of India
The Semiconductor Integrated Circuits Layout Design Registry

निर्गमन सं 141/2023

शुक्रवार

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अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन अधिनियम, 2000 के अधीन प्रकाशित
रजिस्ट्रार कार्यालय, अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री, भारत सरकार
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Ministry of Commerce and Industry
बौद्धिक संपदा भवन
Boudhik Sampada Bhawan
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अनुक्रमणिका
INDEX

क. आधिकारिक टिप्पणियां
A. Official Notes

ख. अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री कार्यालय का अधिकार क्षेत्र
B. Jurisdiction of Office of the Semiconductor Integrated Circuits Layout Design Registry

ग. स्वीकृति के पश्चात विज्ञापित आवेदन
C. Applications advertised after acceptance

घ. आवेदन में शुद्धि या संशोधन करने की अधिसूचना
D. Notification of correction or amendment of application

प्रस्तावना

अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री 1 मई, 2011 से सेमीकंडक्टर एकीकृत परिपथ अभिन्यास डिजाइन अधिनियम, 2000 के अंतर्गत चालू की गई है। अधिनियम के अंतर्गत प्रावधानों के अनुसार अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन जनरल का प्रकाशन अपेक्षित है। इस जनरल का प्रकाशन महीने के दूसरे शुक्रवार कार्य दिवस पर किया जाएगा। इस जनरल से संबंधित सभी पूछ-ताछ अथवा कोई भी अन्य अपेक्षित सूचना रजिस्ट्रार, अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री को संबोधित की जा सकती है। किसी भी प्रकार के सुझावों तथा टिप्पणियों का स्वागत है।

(प्रो. (डॉ.) उन्नत पी. पंडित)
रजिस्ट्रार

INTRODUCTION

The Semiconductor Integrated Circuits Layout-Design Registry has been made operational w.e.f. 1st May 2011 under the Semiconductor Integrated Circuits Layout-Design Act, 2000. In accordance with the provisions under the Act "The Semiconductor Integrated Circuits Layout-Design Journal" is required to be published. This Journal is being published on the 2nd working Friday of the month. All the enquiries related to this Journal or any other information as required should be addressed to the Registrar, Semiconductor Integrated Circuits Layout-Design Registry. Any suggestions and comments are welcome.

(Prof. (Dr) Unnat P. Pandit)
REGISTRAR

- क. आधिकारिक टिप्पणियां
A. Official Notes

अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन आवेदन के पंजीकरण से संबंधित कोई भी जानकारी सभी कार्य-दिवसों में अपराह्न 3.00 से 4.00 के बीच प्राप्त की जा सकती है ।

(प्रो. (डॉ.) उन्नत पी. पंडित)
रजिस्ट्रार

All the queries relating to registration of Semiconductor Integrated Circuits Layout Design may be obtained from the Registry between Timing 3:00 PM to 4:00 PM all working days.

(Prof. (Dr) Unnat P. Pandit)
REGISTRAR

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- ख. अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री कार्यालय का अधिकार क्षेत्र
B. Jurisdiction of Office of the Semiconductor Integrated Circuits Layout Design Registry

अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री (एस. आई. सी. एल. डी. आर.) का मुख्य कार्यालय, बौद्धिक संपदा भवन, प्लॉट नं ३२, सेक्टर १४, द्वारका, नई दिल्ली – 110075 में स्थित है। इसकी राज्यक्षेत्रीय परिसीमाएं जिसके भीतर अर्धचालक एकीकृत परिपथ अभिन्यास डिजाइन रजिस्ट्री का कार्यालय अपने कृत्य कर सकेगा, सम्पूर्ण भारत पर है।

(प्रो. (डॉ.) उन्नत पी. पंडित)
रजिस्ट्रार

The Semiconductor Integrated Circuits Layout-Design Registry (SICLDR) has its head office located in the Boudhik Sampada Bhawan, Plot no. 32, Sector – 14, Dwarka, New Delhi-110075. The territorial limits within which such office of the Semiconductor Integrated Circuits Layout-Design Registry may exercise its functions shall be the whole of India.

(Prof. (Dr) Unnat P. Pandit)
REGISTRAR

- ग. स्वीकृति के पश्चात विज्ञापित आवेदन – दो *
C. Applications advertised after acceptance – Two *

Application Received for Registration under Semiconductor Integrated Circuits
Layout Design Act 2000

Semiconductor Integrated Circuits Layout Design (SICLD) Registry has received an application for registration of LOW CURRENT DRIVER LOGIC USING CUSTOMIZED GATE WITH ON E/D MODE GAAS PHEMT STRUCTURES, Application no: LD-1/12/2021 in the name of M/s Bharat Electronics Limited, Bharat Electronics Limited, Corporate Office, Outer Ring Road, Nagavara, Bangalore-560045, India. Details of the applications are as below:

1. **Date of Receipt for registration of layout design:** 25/01/2021.
2. **Brief Description of the layout design:** The driver logic is fabricated on 0.25um GaAs E/D (Enhancement/ depletion) process using custom designed FET structures to achieve low current less than 1.5mA per individual bit and size 300 X 300 um per bit and 8-bit low Current control logic design with die size of 3.3 X 1.4 mm.
By the use of this process results in reduction in current consumption by using E/D (Enhancement/ depletion) mode of FETs and offers ease of integration. Single bit driver logic cell can be reusable depends on the control bit of RF switches.
As shown in Figure 1, Pad numbers 1 to 8 represents TTL control inputs & 9A to 16B represents 16 complement Output voltage respectively and all supply pads with ESD (electrostatic discharges) protection and on chip by pass capacitor.
3. **Whether the layout design has been commercially exploited:** No
4. **The Address of the office of the registry where the application is filed:** SICLD Registry, Boudhik Sampada Bhawan, Plot No. 32, Sector-14, Dwarka, New Delhi - 110078.

Anyone willing to oppose the filing of the application by M/s Bharat Electronics Limited, Bharat Electronics Limited, Corporate Office, Outer Ring Road, Nagavara, Bangalore-560045, India, may kindly send their application to the SICLD Registry Boudhik Sampada Bhawan, Plot No. 32, Sector-14, Dwarka, New Delhi - 110078.

A notice of opposition to the registration of a layout design under sub section (1) of section 11 shall be given in triplicate on Form LD-2 accompanied by prescribed fee within three months from the date of advertisement of the application for registration in the journal (www.sicldr.gov.in). The notice shall include a statement of the grounds on which the opponent objects to the registration.

To obtain details how to apply, please visit website: www.sicldr.gov.in
Duly filled Application Form may please be sent to: **Registrar**

Semiconductor Integrated Circuits Layout Design Registry, Department for Promotion of Industry and Internal Trade, Ministry of Commerce & Industry (Government of India)
Boudhik Sampada Bhawan, Plot No. 32, Sector-14, Dwarka, New Delhi - 110078

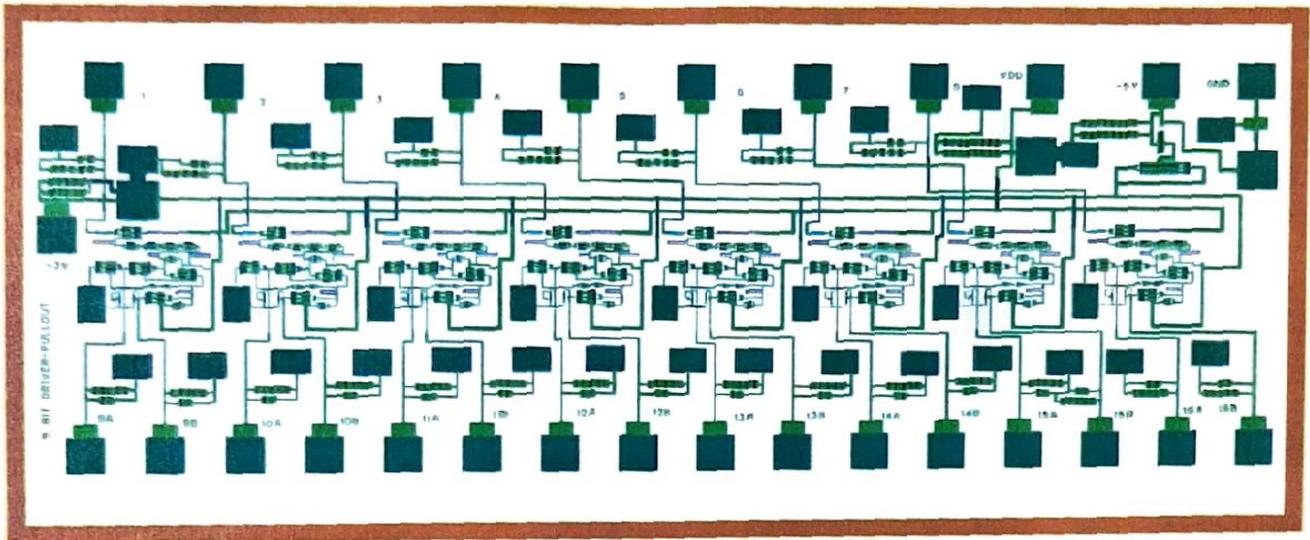
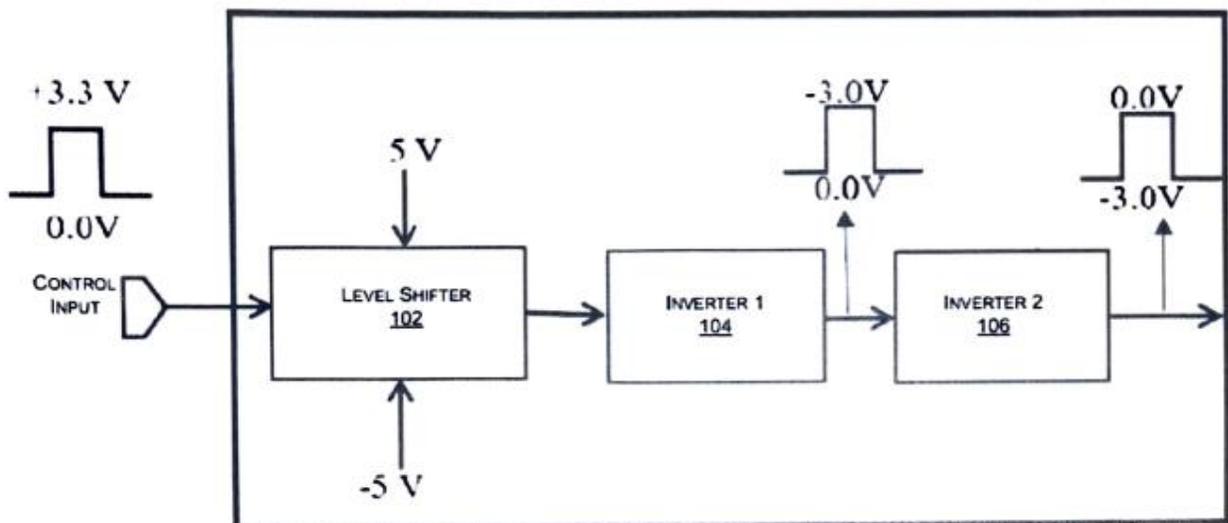


Fig 1. Eight- bit Driver Logic

100 ↘



Application Received for Registration under Semiconductor Integrated Circuits
Layout Design Act 2000

Semiconductor Integrated Circuits Layout Design (SICLD) Registry has received an application for registration of BETTER IIP3, LOW INSERTION PHASE SHIFT, WELL MATCHED S-BAND 7-BIT GAAS MMIC DIGITAL ATTENUATOR, Application no: LD-1/13/2021 in the name of M/s Bharat Electronics Limited, Bharat Electronics Limited, Corporate Office, Outer Ring Road, Nagavara, Bangalore-560045, India. Details of the applications are as below:

1. **Date of Receipt for registration of layout design:** 08/03/2021.
2. **Brief Description of the layout design:** This layout connected to better IIP3, low insertion phase shift S-band 7-bit GaAs MMIC digital attenuator using 0.25um InGaAs Technology. Layout consists of cascaded seven attenuation bits, with a total die dimension of 2.6 x 2.5 x 0.1 mm in X, Y and Z direction. 0.25-dB and 0.5-dB attenuation bits are realized using simple shunt topology. 1-dB, 2 dB, 4-dB and 8-dB attenuation bits are implemented using switched T-topology. 16-dB attenuation bit is Single Pole Double Throw (SPDT) topology to achieve better attenuation flatness over 3 to 3.6 GHz. ESD diodes are added to control lines and supply lines to protect die from ESD damage. (ESD protection circuits on control & supply lines are starts with "EP"). D2 process switches are used in all transistors (Starts with T), TFR resistors (Starts with TR) - are used in realizing attenuation values and on control lines near DC-RF crossovers, MESA resistors (Starts with M) are used in Gate resistor realization, DC Blocking capacitors are included in the design to avoid the requirement of external blocking capacitors, EPI resistors (El) also used to realize resistor on control line near DC-RF cross over. Two ~5302 resistors in series are used in transmission line crossovers. ~3002 resistors are used in lengthy transmission lines. 5KQ MESA resistor to Ground in transmission line will ensure proper transistor switching with respect to digital control signals. All capacitors in this design are MIM capacitor (Starts with C) with capacitance density 600pF/ sq.mm. Resistors used are TFR, MESA and EPI resistor with resistivity 5002 /sq. 13092 /sq and 3102 /sq respectively. Attenuator has inbuilt driver logics (Starts with D), which operates with +SV, -5V and control TTL signal to change states from 0 to 127.
3. **Whether the layout design has been commercially exploited:** No
4. **The Address of the office of the registry where the application is filed:** SICLD Registry, Boudhik Sampada Bhawan, Plot No. 32, Sector-14, Dwarka, New Delhi - 110078.

Anyone willing to oppose the filing of the application by M/s Bharat Electronics Limited, Bharat Electronics Limited, Corporate Office, Outer Ring Road, Nagavara, Bangalore-560045, India, may kindly send their application to the SICLD Registry Boudhik Sampada Bhawan, Plot No. 32, Sector-14, Dwarka, New Delhi - 110078.

A notice of opposition to the registration of a layout design under sub section (1) of section 11 shall be given in triplicate on Form LD-2 accompanied by prescribed fee within three months from the date of advertisement of the application for registration in the journal (www.sicldr.gov.in). The notice shall include a statement of the grounds on which the opponent objects to the registration.

To obtain details how to apply, please visit website: www.sicldr.gov.in

Duly filled Application Form may please be sent to: **Registrar**

Semiconductor Integrated Circuits Layout Design Registry, Department for Promotion of Industry and Internal Trade, Ministry of Commerce & Industry (Government of India)

Boudhik Sampada Bhawan, Plot No. 32, Sector-14,
Dwarka, New Delhi - 110078

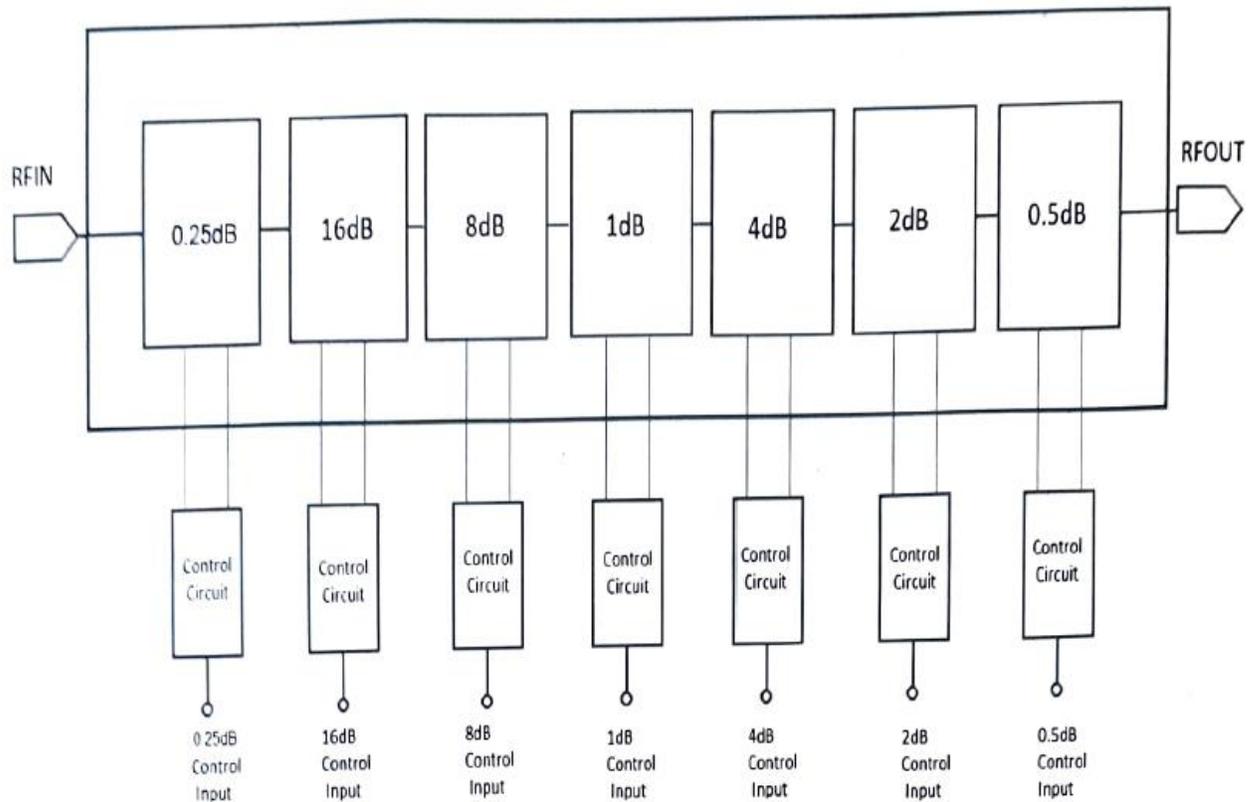


Fig -1: SCHEMATIC DIAGRAM OF S-BAND 7-BIT GaAs MMIC DIGITAL ATTENUATOR

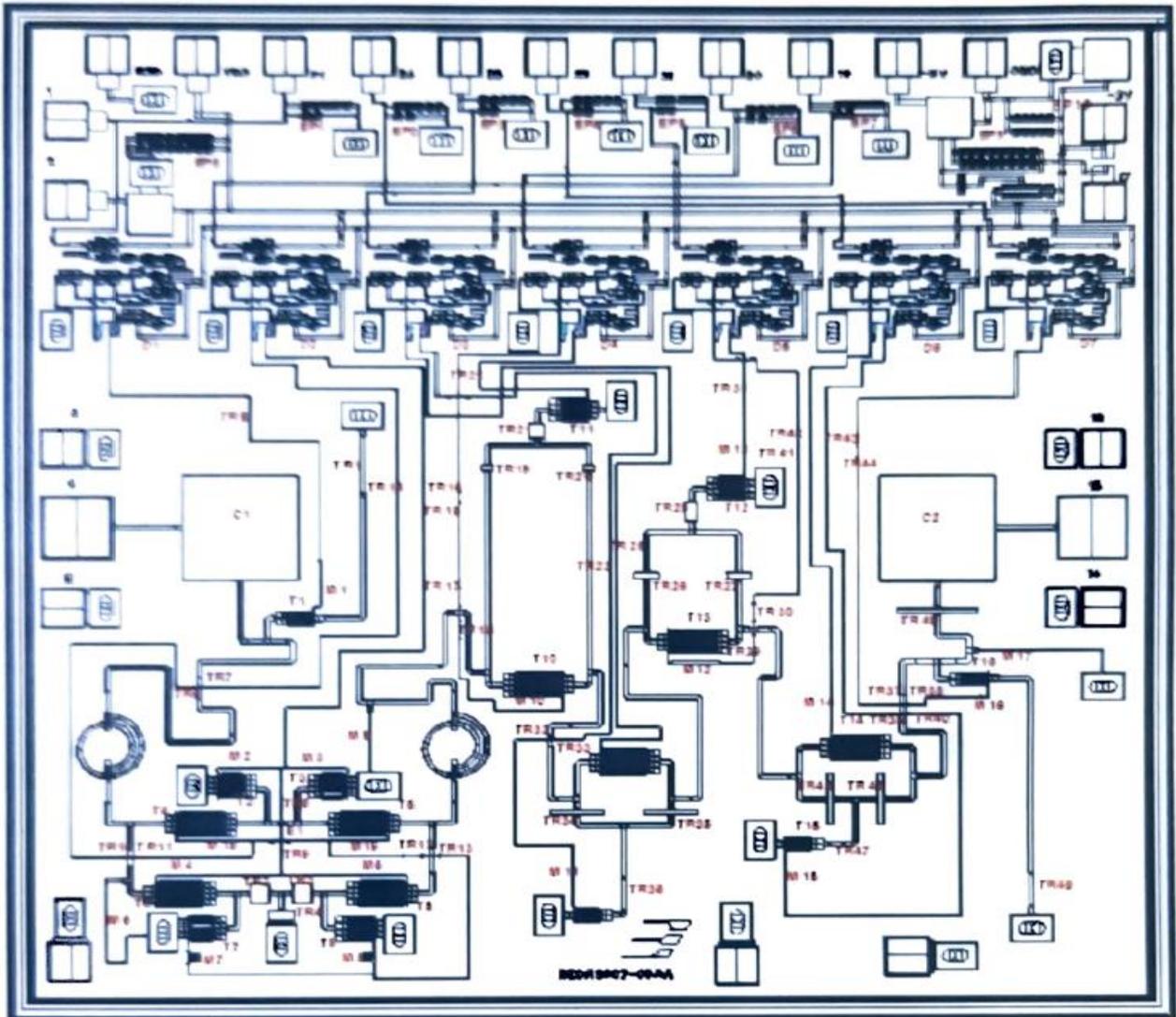
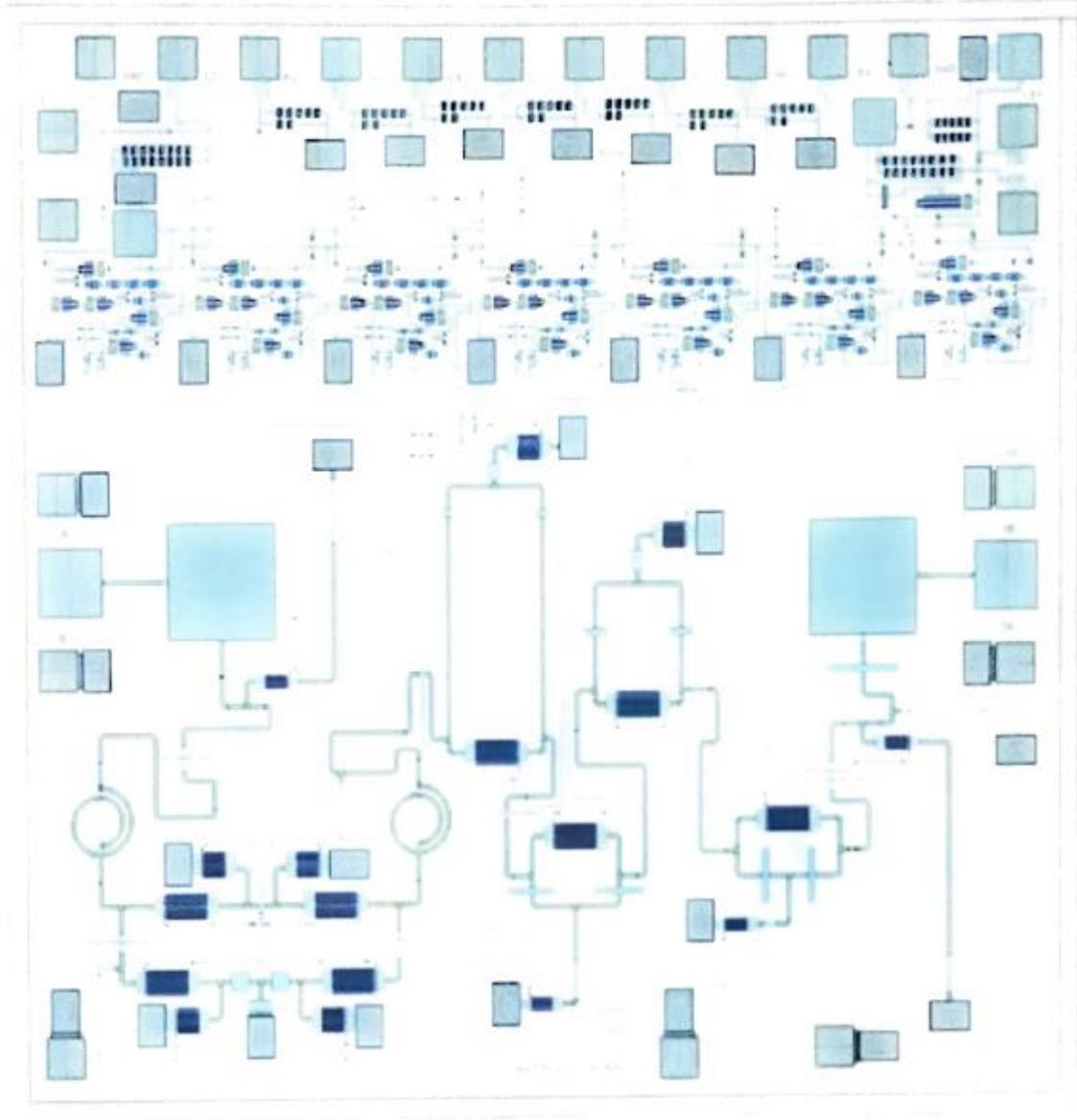


Fig I. Sband 7-bit digital attenuator



*दो आवेदन प्राप्त हुआ।
*two application received.

- घ. आवेदन में शुद्धि या संशोधन करने की अधिसूचना - शून्य
D. Notification of correction or amendment of application - Nil